BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates in general to a semiconductor device, such as an MOS transistor, in which there is compensation for the drop in the threshold voltage (V_{th}) due to the short-channel effects, and to a process for fabrication of such a semiconductor device.

2. DESCRIPTION OF THE RELATED ART

For a given nominal channel length (L) of a transistor, the threshold voltage (V_{th})drops suddenly, in particular for short-channel transistors (i.e., those having a channel length of less than 0.25 μm and typically a channel length, L, of about 0.18 μm).

The threshold voltage of a semiconductor device such as an MOS transistor, in particular a short-channel device, is a critical parameter of the device. This is because the leakage current of the device (for example, of the transistor) depends strongly on the threshold voltage. Taking into consideration current supply voltages and those envisaged in the future (from 0.9 to 1.8 volts) for such devices and the permitted leakage currents (I_{off} of approximately 1 nA/μm), the threshold voltage V_{th} must have values of approximately 0.2 to 0.25 volts.

The sudden voltage drop (or roll-off) in the zones of the channel region of the semiconductor device results in dispersion of the electrical characteristics of the device and makes it difficult to obtain the desired threshold voltages.

To remedy this threshold voltage roll-off in semiconductor devices such as MOS transistors, it has been proposed, as described in the article "*Self-Aligned Control of Threshold Voltages in Sub-0 .2-μm MOSFETs*" by Hajima Kurata and Toshihiro Sugii,

IEEE Transactions on Electron Devices, Vol. 45, No. 10, October 1998, to form, in the channel region, pockets adjacent to the source and drain region junctions that have a conductivity of the same type as the substrate; but in which, the dopant concentration is greater than that of the substrate.

Although this solution reduces the threshold voltage roll-off gradient in the channel region, the short-channel effects lead to a more rapid roll-off of the threshold voltage, V_{th}, than the increase in the threshold voltage that can be obtained by incorporating the compensation pockets of the prior art.

Consequently, although these compensation pockets allow partial local compensation for the roll-off of the threshold voltage, V_{th}, it is not possible to obtain complete compensation for the roll-off over the entire channel region range desired.

Therefore a semiconductor device, such as an MOS transistor, that remedies the drawbacks of the devices of the prior art may be desired.

More particularly, a semiconductor device, such as an MOS transistor, whose voltage threshold roll-off due to the short-channel effects is almost fully compensated for may be desired. This makes it possible to achieve channel lengths which are arbitrarily small but non-zero.

Also a semiconductor device, such as an MOS transistor, may have a constant threshold voltage, V_{th}, when the channel length, L, decreases down to very small effective channel lengths, for example, 0.025 μm or less.

A process for fabricating a semiconductor device may apply to devices having channels of arbitrarily small length, these being, moreover, technologically realizable.

DESCRIPTION OF THE INVENTION

A semiconductor device is described that may have a semiconductor substrate with a predetermined concentration, Ns, of a dopant of a first conductivity type. The device may have source and drain regions which are doped with a dopant of a second conductivity type, which is opposite of the first conductivity type. Junctions delimiting a channel region of predetermined nominal length, L_N, may be defined in the substrate. A first pocket adjacent to each of the junctions and having a predetermined length, Lp, may be defined. The first pockets may be doped with a dopant of the first conductivity type but with a local concentration, Np, which locally increases the net concentration in the substrate. The device may include at least one second pocket located adjacent to each of the junctions and stacked against each of the first pockets. These second pockets may have a length, Ln, such that $Ln > Lp$. The second pockets may be doped with a dopant of the second conductivity type and have a concentration, Nn, such that $Nn < Np$. This may locally decrease the net concentration of the substrate without changing the conductivity type.

In an embodiment, the second pockets include a plurality of elementary pockets stacked against one another. Each elementary pocket of a given rank, i, may have a predetermined length, Ln_i, and a predetermined concentration, Nn_i, of a dopant of the second conductivity type satisfying the following relationships:

$Ln_1 > Lp$,

$Ln_{i-1} < Ln_i < Ln_{i+1}$,

$Nn_{i-1} > Nn_i > Nn_{i+1}$, and

the sum, ΣNn_i, of the concentrations of the dopant of the second conductivity type in the elementary pockets may be such that:

$\Sigma Nn_i < Ns$.

In other words, the second pockets decrease the net concentration of dopant of the first conductivity type both in the first pockets and in the channel region. However, they do not change the conductivity type of the first pockets nor of the channel region.

A process for fabricating a semiconductor device as defined above is described. The process may include the formation of a source region and of a drain region in a semiconductor substrate having a predetermined concentration, Ns, of a dopant of a first conductivity type. The source region and the drain region may be doped with a dopant of a second conductivity type, which is opposite of the first conductivity type. The source and drain regions may form one or more junctions in the substrate such that the junctions delimit between them a channel region. The channel region may have a predetermined nominal length, L_N. In the channel region in a zone adjacent to each of the junctions, one or more first pockets may be formed having a predetermined length, Lp, and a predetermined concentration, Np. This may locally increase the net concentration in the substrate above Ns. The process may furthermore include the implantation, in the channel region, of a dopant of the second conductivity type, which is opposite of the first conductivity type. This may be done under a set of conditions such that at least one second pocket is formed in the channel region. Each second pocket may be stacked against each of the first pockets, respectively. The second pocket may have a length, Ln, such that Ln > Lp, and a concentration, Nn, of a dopant of the first type such that Nn < Np. This may locally decrease the net concentration in the substrate, without changing the conductivity type.

In a preferred embodiment, the implantation of the dopant of the second conductivity type consists of a series of successive implantations under a set of conditions such that the second pockets formed each consist of a plurality of elementary pockets stacked against one another. Each elementary pocket of a given rank, i, may have a length, Ln_i, and a concentration, Nn_i, of a dopant of the second conductivity type satisfying the relationships:

$Ln_1 > Lp$,

$Ln_{i-1} < Ln_i < Ln_{i+1}$,

$Nn_{i-1} > Nn_i > Nn_{i+1}$, and

the sum, ΣNn_i, of the concentrations of the dopant of the second conductivity type in the elementary pockets being such that:

$\Sigma Nn_i < Ns$.

The lengths Lp and Ln of the pockets are taken from the junctions.

Implantation of a dopant in a semiconductor substrate is a known process and it is possible, in the present process, to use any implantation process conventionally used in the technology of semiconductors.

As is known, the formation of doped pockets in a semiconductor substrate depends on the angle of incidence of the implantation with respect to the normal to the substrate, on the implantation dose, and on the implantation energy of the dopant. Thus, by varying the angle of incidence and the dopant dose, it is possible to increase the length of the implanted pocket and to vary the dopant concentration.

As a variant, in order to vary the length of the second implanted pockets and their dopant concentration, successive implantation steps may be carried out with the same angle of incidence with respect to the normal, the same dose, and the same implantation energy. However, subjecting the device to a different annealing heat treatment step after each successive implantation step may make the dopant implanted in the substrate diffuse differently for each implanted pocket.

BRIEF DESCRIPTION OF THE DRAWINGS

The remainder of the description refers to the appended figures, which show respectively:

Figure 1, a first embodiment of a semiconductor device, such as an MOS transistor;

Figure 2, a second embodiment of a semiconductor device; and

Figure 3, a graph of the threshold voltage (V_{th}) for various semiconductor devices as a function of the effective channel length.

DETAILED DESCRIPTION OF THE DRAWINGS

Figure 1 shows a first embodiment of a semiconductor device, such as an MOS transistor. The semiconductor device may include a semiconductor substrate 1, which may be, for example, a silicon substrate doped with a dopant of a first conductivity type (for example, p-type conductivity). Source 2 and drain 3 regions may be formed in the substrate 1 and doped with a dopant of a second conductivity type, which is opposite of the first conductivity type (for example, an n-type dopant). The source and drain regions may, in the substrate, define junctions 4, 5 delimiting between them a channel region 6.

The channel region 6 may be covered with a gate oxide layer 11 (for example, a thin silicon oxide layer), which is itself surmounted by a gate 12 (for example, a gate made of silicon). The gate 12 may be flanked on two opposed sides by spacers 13, 14 made of a suitable dielectric.

To reduce the rate of roll-off of the threshold voltage, V_{th}, in the channel region 6, two first pockets 7, 8 are formed in the channel region. Each pocket may be adjacent to one of the junctions 4, 5, respectively. These pockets are doped by means of a dopant of the first conductivity type, p, but with a concentration, Np, of dopant which locally increases the concentration in the substrate to above Ns and has a length, Lp, as short as possible.

Two second pockets 9, 10 are formed in the channel region 6. The second pockets are each stacked against one of the first pockets, but with a length, Ln, greater than the length, Lp, of the first pockets. The second pockets are doped with a dopant of the second conductivity type. For example, the dopant may be an n-type dopant with a concentration, Nn, such that Nn is less than the concentration Np of dopant of the first conductivity type in the substrate.

Thus, in the zones of the second pockets, the net concentration of dopant of the first conductivity type (for example, the p-type dopant) is decreased but the nature of the

conductivity in the channel region is not changed. The channel may still remain a region of p-type conductivity.

Figure 2, in which the same reference numbers denote the same elements as previously, shows another embodiment of a semiconductor device. Figure 2 shows that the second pockets 9, 10 may include pluralities of elementary pockets stacked against one another. For example, pluralities of elementary pockets may include three elementary pockets as shown in the embodiment in Figure 2.

Each elementary pocket of a given rank, i, has a length, Ln_i, and a concentration, Nni, of dopant of the second conductivity type which satisfy the following relationships:

$Lp < Ln_i$,

$Ln_{i-1} < Ln_i < Ln_{i+1}$,

$Nn_{i-1} < Nn_i < Nn_{i+1}$, and

the sum ΣNn_i of the concentrations of dopant of the second conductivity type in the elementary pockets being such that:

$\Sigma Nn_i < Ns$.

In other words, the elementary pockets stacked against the first pockets 7 and 8 are also stacked against one another. However, they have increasing lengths and, concurrently, concentrations of dopant of the first conductivity type which decrease as their lengths increase.

Moreover, the sum of the concentrations, ΣNn_i, of the stacked elementary pockets is such that it remains less than the concentration, Ns, of dopant of the first conductivity type in the substrate so that the conductivity type of the channel region 6 is not modified.

Thus, in the case shown in figure 2, in which the second pockets consist of three elementary pockets. The lengths and dopant concentrations of the elementary pockets satisfy the relationships:

$Lp < Ln_1$,

$Ln_1 < Ln_2 < Ln_3$,

$Nn_1 > Nn_2 > Nn_3$, and

$Nn_1 + Nn_2 + Nn_3 < Ns$.

Figure 3 shows simulated graphs of the threshold voltage, V_{th}, for transistors having a gate oxide layer 4 nm in thickness and for a drain/source voltage of 1.5 volts as a function of the effective channel length. The lengths, Lp, and the concentrations, Np, of the first pockets doped with a dopant of the same type as the substrate correspond to the minimum channel length to be obtained and the highest doping.

Curve A corresponds to the stacking of a single second pocket and shows that a flat V_{th} is obtained for a channel length down to 0.15 μm.

Curve B corresponds to the stacking of two second pockets and shows that a flat V_{th} is obtained for a channel length down to 0.07 μm.

Finally, curve C corresponds to the stacking of seven second pockets and shows that a flat V_{th} can be obtained for a channel length down to 0.025 μm.

Thus, the above curves show that the necessary doping levels remain reasonable and make it possible to obtain flat curves of V_{th} as a function of the effective channel length down to effective lengths of 25 nm. This may be so even with gate oxide thicknesses of 4 nm.